REMARKS

By this amendment, claims 4 and 13 have been cancelled and claims 1-3, 5-12, and 14-20 have been amended in the application. Currently, claims 1-3, 5-12, and 14-20 are pending in the application.

The Examiner stated that the drawings were objected to because of some minor spelling errors. By this amendment, the words "Hoffman" and "Decording" in Fig. 6 have been amended to the terms "Huffman" and "Decoding". Also, the term "Hoffman" in Fig. 12 has been amended to "Huffman". Also, the terms "Encording" and "Decording" in Fig. 17 have been amended to "Encoding" and "Decoding". It is respectfully submitted that this objection has been overcome and should be withdrawn.

The Examiner stated that the disclosure was objected to and applicants were requested to change all references to "Hoffman" in the specification to "Huffman". By this amendment, the word "Hoffman" throughout the specification has been amended to the word "Huffman". It is respectfully submitted that this objection has been overcome and should be withdrawn.

The Examiner also stated that a new title was required. The Examiner suggested the following title: "Parallel Signal Processing Device for a Portable Audio System". By this amendment, the title has been changed to "Parallel Signal Processing Device for a Portable Audio System" as the Examiner suggested. It is respectfully submitted that objection has been overcome and should be withdrawn.

Claims 9 and 18 were rejected under 35 USC 112, second paragraph. The Examiner believed that claims 9 and 18 recite the limitation "said first process" in the respective fifth lines of each claim, along with "said second process" in the respective eleventh and twelfth lines of each claim and these terms lacked antecedent basis. By this amendment, claims 9 and 18 have been amended to provide antecedent basis by reciting "a first process" and "a second process". It is therefore respectfully submitted that this rejection has been overcome and should be withdrawn.

Claims 1-2, 9-11 and 18 were rejected under 35 USC 102(b) as being anticipated by Hall, Jr. (U.S. Patent No. 4,351,025).

The Examiner stated that Hall, Jr. disclosed a parallel digital processor architecture that involves the use of a master central processing unit (MC) and a plurality of parallel elemental computers (ECs) (column 2, lines 41-60). The Examiner

believed that the phrase "first to Nth sub signal processing sections each of which is given (N x t + i)th frame signals" of the phrase "a first digital signal framed for each predetermined time interval" as well as the phrase "each of which completes a first process within a period (N x T)" read on the operations of the Hall, Jr., circuit arrangements and the ECs. The Examiner also believed that the phrase "a main signal processing section which converts a signal processed in said (i + 1)th sub signal processing section into a second digital signal by completing a second process within a period T" read on that the MC controls the data transfer among the ECs and also performs logic operations as depicted in Fig. 4 and performs a function for a period less than that used by the ECs (column 1, lines 64-68 and column 2, lines 1-5).

This rejection is respectfully traversed in view of the amendments to the claims and the following remarks.

The present invention relates to a signal processing device and a signal processing method performing a compressing/decoding process for an audio signal, and more specifically to a signal processing device and method in which the power consumption is reduced by making the processing parallel.

FIG. 5 shows a configuration of a signal processing device according to the present embodiment. This signal processing device has one main signal processing section 10 and first to third sub signal processing sections 11 to 13. A distribution section 14 distributes a frame signal of the input to one of the sub signal processing sections 11 to 13 in accordance with a frame number. A selection section 15 selects one of the sub signal processing sections 11 to 13 in accordance with the frame number to send it to the main signal processing section 10. A frame number management section 16 updates the frame number each time one frame period T elapses to give the number to the distribution section 14 and the selection section 15. Here, it is supposed that the respective sub signal processing sections 11 to 13 have the capabilities to process the first process A within the time period 3 × T, and the main signal processing section 10 has the capability to process the process B within the time period T.

Here, since the first process A has to start the process of the next frame time before the processing of the past frame time is completed, the process A is a non-chain process, that is, a process in which the information generated in the past frame time is not employed. Conversely, the second process B can be a

process in which the information generated in the past frame time is employed, that is, a chain process. This is because the processing of the next frame time is always started after the processing of the past frame time is completed.

FIG. 8 is a view showing a flow of the processing of the signal processing device of the present embodiment in the order of time. In the first frame time, the first frame signal is inputted to the second sub signal processing section 12, and for this signal the process A [1] is started so that this process is completed within the period 3T. In the second frame time, the second frame signal is inputted to the third sub signal processing section 13, and for this signal the process A [2] is started so that this process is completed within the period 3T. In the third frame time, the third frame signal is inputted to the first sub signal processing section 11, and for this signal the process A [3] is started. At the same time in the main signal processing section 10, the process B [0] is started for the output signal from the first sub signal processing section 11 so that this process is completed within the period T.

By repeating this type of processing for each frame time one after another, the signal processing composed of the process A and the process B is performed for the frame signals inputted at

the time T intervals so that the output frame signals are generated at the time T intervals. At this time, as can be seen from FIG. 8, in the main signal processing section 10 and the sub signal processing sections 11 to 13, the processing can be made parallel without dead time.

Since the processing employing the information generated in the past frame time is excluded in the first process A, the need to deliver a signal between the respective sub signal processing sections is eliminated, whereby the parallel processing can be efficiently performed.

In the present embodiment, since the processing amount of the process A is three times the processing amount of the process B, three sub signal processing sections are provided. Efficient parallel processing can be performed if N sub signal processing sections are provided when the processing amount of the process A is N times (N is a natural number) the processing amount of the process B.

As described above, in the present embodiment, when the processing composed of the process A and the process B is parallel processed, even if there is a deviation in throughputs of the process A and the process B, parallel processing can be performed efficiently.

FIG. 11 shows a configuration of a signal processing device according to the present embodiment. The signal processing device has one main signal processing section 50 and first to third sub signal processing sections 51 to 53. A distribution section 54 distributes an output signal from the main signal processing section 50 to one of the sub signal processing sections 51 to 53 in accordance with the frame number. A selection section 55 selects the output signal of one of the sub signal processing sections 51 to 53 in accordance with the frame number to output it. A frame number management section 56 updates the frame number each time one frame period T elapses to give it to the distribution section 54 and the selection section 55. Here, it is supposed that the main signal processing section 50 has the capability to process the first process A within the time period T, and the respective sub signal processing sections 51 to 53 have the capabilities to process the process B within the time period (3 × T).

Here, since with respect to the second process B, the process of the next frame time has to be started before the processing of the past frame time is completed, the process B is the non-chain process. Conversely, the first process A can be the chain process. This is because the processing of the next

frame time is started after the processing of the past frame time is completed.

FIG. 14 is a view showing the flow of time for processing in the signal processing device. Operations of this signal processing device are described with relation to FIG. 11.

First, in the main signal processing section 50, the process A is performed for the input frame signal within the period T.

Then, the distribution section 54 sends the output signal from the main signal processing section 50 to the (i + 1)th sub signal processing section when the frame number shown by the frame number management section 56 is (N x t + i)(t and i are integers, N is a natural number and $t \geq 0$, and $0 \leq i < N$).

In the sub signal processing sections 51 to 53, the process B is executed for the after-process A signal that is distributed within the time period 3T.

Independent claim 1 has been amended to recite "wherein the second process contains a process employing information generated in a past frame time; and the first process excludes the information generated in the past frame time."

Independent claim 9 has been similarly amended to recite "the first process excluding information generated in a past frame time". Also, independent claim 9 has been similarly

amended to recite "the second process using the information generated in the past frame time."

Independent claim 10 has been similarly amended to recite "wherein said first process excludes information generated in a past frame time; and said second process using the information generated in the past frame time."

Likewise, independent claim 18 has been amended to recite "the first process excluding information generated in a past frame time". Also, independent claim 18 has been similarly amended to recite "the second process employing the information generated in the past frame time".

These features are not shown in Hall, Jr. or the prior art of record.

Hall, Jr. relates to a parallel digital computer architecture and more particularly, to a computer for performing programs digitally but in the format of an analog computer.

Hall, Jr. discloses that the parallel digital computer (PDC) includes a plurality of elemental computers (ECs), typified by a state-of-the-art microprocessor, interconnected through a master computer (MC) and its memory, and synchronized to a real-time clock (RTC). A master computer central processing unit (MC CPU) 1, MC memory 2 and multiple ECs 3 communicate by means of a data

bus 4 and an address bus 6. The actual distribution of data registers between the MC memory 2 and the individual ECs can be lumped in the MC memory or distributed among the ECs; in either case they are treated as being shared.

Hall, Jr. also discloses that the minimum frame time (FT) is primarily a tradeoff between the number and duration of the EC time segments with the remainder allocated to the MC and the interrupt delays. The major time consumers in each FT are the EC segments.

Hall, Jr. also discloses that the PDC architecture discloses sequential processing and transfer of data from EC to EC, with the MC CPU designating the ECs to operation and the path of the data transfer. Since each EC must, in turn during its time segment, act upon the data processed by the previous EC during the previous EC time segment, and all intermediate EC processed data must be available to the integrator EC in each FT, the maximum number of series connected non-integrator ECs between successive in series integrator ECs is one less than the number of EC time segments in each FT.

Hall, Jr. does not disclose that first to Nth sub signal processing sections each of which is given (N × t + i)th frame signals (i and t are integers, N is a natural number, and

$0 \leq i < N$) of a first digital signal framed for each predetermined time interval and each of which completes a first process within a period ($N \times T$) (T is a real number); a main signal processing section which converts a signal processed in a $(i + 1)$th sub signal processing section into a second digital signal by completing a second process within a period T as recited in claim 1.

Hall, Jr. also does not disclose that the second process contains a process employing information generated in a past frame time; and the first process excludes the information generated in the past frame time as recited in claim 1.

Hall, Jr. also does not disclose that the first process excluding information generated in a past frame time and Hall, Jr. also does not disclose that the second process using the information generated in the past frame time as recited in claim 9.

Hall, Jr. also does not disclose that the first process excludes information generated in a past frame time; and the second process using the information generated in the past frame time as recited in claim 10.

Hall, Jr. also does not disclose that the first process excluding information generated in a past frame time and Hall, Jr. also does not disclose that the second process employing the information generated in the past frame time as recited in claim 18.

Therefore, applicants respectfully submit that independent claims 1, 9, 10 and 18 clearly define over Hall, Jr. and this rejection should be withdrawn. Regarding dependent claims 2-3, 5-8, 11-12, and 14-16, applicants submit that these claims are also allowable in view of their amendments and the amendments that have been made to independent claims 1, 9, 10 and 18.

Claims 1-2, 4, 8-11, 13 and 17 and 18 were rejected under 35 USC 103(a) as being obvious over Ahamed et al. (U.S. Patent No. 5,978,831). Claims 3 and 12 were rejected under 35 USC 103(a) as being obvious over Ahamed et al. as applied above and in further view of Matt et al. (U.S. Patent No. 6,581,153). Claims 5-7 and 14-16 were rejected under 35 USC 103(a) as being obvious over Ahamed et al. as applied above, and in further view of the applicants admitted prior art. Claims 19 and 20 were rejected under 35 USC 103(a) as being obvious over Ahamed et al. as applied above, and in further view of well-known prior art.

These rejections are respectfully traversed in view of the amendments to the claims and the following remarks.

Ahamed et al. relates to the architecture of multiprocessor computers. Ahamed et al. disclose two processors where the clock rate of one is an integer multiple of the other, and it is generalized to multiple processors with fractional relationships between the clock rates.

Ahamed et al. also disclose the illustrative example of FIG. 1, where the faster processor 12 operates at three times the rate of the slower processor 11. The timing diagram for the arrangement of FIG. 1 is shown in FIG. 2. The top time line in FIG. 2 shows the arrival times of data blocks 16. Each of the subsequent time lines shows the progression of individual data blocks 16 of a frame 15 through the arrangement of FIG. 1.

Ahamed et al. also disclose that in pipelined architectures in FIGs. 1, 4, 7 and 10 become the building blocks in the pipeline. The pipeline can be visualized as a chain of various production stages in which the completion time of all of the stages is uniform. Multiple processors of varying rates can be freely used to construct any or each production stage in the pipeline.

However, applicants respectfully submit that Ahamed et al. do not disclose that a main signal processing section which converts a signal processed in a (i + 1)th sub signal processing section into a second digital signal by completing a second process within a period T as recited in claims 1, 19 and 20.

Ahamed et al. also do not disclose that the second process contains a process employing information generated in a past frame time; and the first process excludes the information generated in the past frame time as recited in claim 1.

Ahamed et al. also do not disclose that the first process excluding information generated in a past frame time and Ahamed et al. also do not disclose that the second process using the information generated in the past frame time as recited in claim 9. Ahamed et al. also do not disclose that converting a signal processed in a (i + 1)th sub signal processing section into the second digital signal by completing a second process within a period T in the main signal processing section as recited in claim 9.

Ahamed et al. also do not disclose that the first process excludes information generated in a past frame time; and the second process using the information generated in the past frame time as recited in claim 10. Ahamed et al. also do not disclose

that a main signal processing section which is given (N × t + i)th frame signals (i and t are integers, N is a natural number, and $0 \leq i < N$) of a first digital signal framed for each predetermined time interval and which completes a first process within a period T (T is a real number) as recited in claim 10.

Ahamed et al. also do not disclose that the first process excluding information generated in a past frame time and Ahamed et al. also does not disclose that the second process employing the information generated in the past frame time as recited in claim 18. Ahamed et al. also do not disclose that converting a (N + 1)th frame signal processed by said main signal processing section and given to said first to Nth sub signal processing sections one after another, into said second digital signal by completing a second process within a period (N × T) in the first to Nth sub signal processing sections as recited in claim 18.

Also, applicants respectfully submit that Ahamed et al. does not teach or suggest the usage of a pipelined multi-processor and the replaced single processor.

Therefore, applicants respectfully submit that Ahamed et al. and other cited references, individually or in combination, do not teach or suggest the presently claimed features. Further,

applicants respectfully submit that one of ordinary skill in the art would not have combined these references to render the claimed invention obvious. Also, there is no teaching or suggestion for the proposed combinations in the applied references.

In view of foregoing amendments and remarks, it is respectfully submitted that the pending claims are allowable over the prior art of record. Thus, applicants respectfully submit that the application is now in condition for allowance and an action to this effect is respectfully requested.

If there are any questions or concerns regarding the amendments or these remarks, the Examiner is requested to telephone the undersigned at the telephone number listed below.

Respectfully submitted,

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